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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/580,929	05/30/2006	Hideo Nagai	50478-2200	9240

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EXAMINER	
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ART UNIT	PAPER NUMBER
2814	

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11/03/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,929	NAGAI, HIDEO	
	Examiner	Art Unit	
	STEVEN H. RAO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 14-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-7 and 14-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05/30/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

2. Applicant's submission filed on August 21, 2009 has been entered and forwarded to the examiner on August 26, 2009.

3. Therefore Claims 1-7 and 14-26 as recited in the amendment accompanying the RCe are pending in the Application.

4. Claims 8 to 13 have been cancelled.

Information Disclosure Statement

No further Ids after the filed on May 30, 2006 have been filed in this case.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21 (2) of such treaty in the English language.

2. Claims 1 to 7 and 14-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Durocher et al. (U.S. Patent Publication No. 2003/0160256, herein after Durocher). (for response to Applicants' arguments-see section below).

With respect to claims 1 and 8 Durocher describes a semiconductor light emitting device comprising: a substrate(fig.9 # 41)(mounting substrate -cl. 8) ; a semiconductor multilayer structure formed on a first main surface of the substrate (FIG. 9 everything on top of 41) the semiconductor multilayer structure including a light emitting layer (fig. 9 # 59) ; a first electrode and a second electrode formed on the semiconductor multilayer structure, power being supplied to the semiconductor multilayer structure through the first electrode and the second electrode causing the light emitting layer to emit light; (fig. 9 # 37,etc.) a phosphor film covering at least a main surface of the semiconductor multilayer structure which faces away from substrate; (fig. 10 # 65) a first terminal and a second terminal formed on a second main surface of the substrate; (figs., wherein

the semiconductor multilayer structure is divided into a plurality of portions by a division groove, (fig.,1) and each of the plurality of portions is an independent light emitting element, (fig.1 #1)

each of a plurality of light emitting elements have a diode structure, and includes an anode electrode and a cathode electrode, (inherent in every diode) and an insulating film is formed on a side surface of each of the plurality of light emitting elements, (fig.9 # 65, para 0066)

the plurality of light emitting elements are connected in series such that a cathode electrode of a light emitting element is connected to an anode electrode of a different light emitting element using a wire formed by a thin metal film formed on the insulating film, (fig. 9- three LEDS fig. 9, figs. E.g. fig.1 connected to different LEDS , wire – figs. E.g. fig. 10 # 61, 63 ,leads –well known to be formed from conductive metal on insulating film figs. 16 # 38 etc.) and one of an anode electrode of one of the plurality of light emitting elements at a higher potential end of an array of the plurality of light emitting elements is the first electrode, (para 0063, inherent every diode has to have either anode or cathode at higher potential for the device to function as diode and emit light).

With respect to claim 2 Durocher describes the semiconductor light emitting device of Claim 1, wherein the semiconductor multilayer structure includes a light reflective layer between the light emitting layer and the one of the plurality of main surface of the substrate. (fig. 10 65 contacts top of 49 i.e. is between 41- substrate and light emitting element 59 and claim 31, figs.)

at least part of each of the first conductive member and the second conductive member is a plated-through hole provided in the substrate. (shown in fig. 4 #51, para 0048).

With respect to claims 3 and 6 Durocher describes the semiconductor light emitting device of Claim 2, wherein the division groove is deep enough to reach the substrate,. (figs.l, fig. 13).

With respect to claims 4 and 7 Durocher describes the semiconductor light emitting device of Claim 1, a first terminal and a second terminal formed on another one of the plurality of main surfaces of the substrate; a first conductive member electrically connecting the first electrode to the first terminal; (fig.9 # 37) and a second conductive member electrically connecting the second electrode to the second terminal (fig. 9 #49, para 0048) wherein the plurality of light emitting elements are formed on locations aside from locations of the plated-through holes. (cl.7- fig. 1, etc.)

With respect to claim 5 Durocher describes the semiconductor light emitting device of Claim 1, wherein at least a plated through hole provided in the substrate.(shown in fig. 4 # 51, para 0048)

With respect to claim 6 Durocher describes the semiconductor light emitting device of Claim 5, wherein each of the plated through holes is located at a different corner of the substrate. (Fig.4 #51,49, para 0049).

With respect to claim 14 Durocher describes the semiconductor light emitting device of Claim 4, wherein at least part of each of the first conductive member and the second conductive member is a conductive film formed on a side surface of the substrate.(fig. 9 # 37,49).

With respect to claims15 and 16 Durocher describes the semiconductor light emitting device of Claim 1, wherein the substrate is highly resistant (plastic- para 0004) and the semiconductor multilayer structure has a structure of epitaxial growth on the substrate.

With respect to claims17 to 23 Durocher describes the semiconductor light emitting device of Claim 1, wherein the semiconductor multilayer structure is a semiconductor multilayer structure that has been epitaxially grown on a single-crystal substrate different from the substrate and transferred to the substrate.(para 0083), wherein the anode electrode for each of the plurality of light emitting elements includes a transparent electrode ,a distributed Bragg reflector layer, (para 0067-1nGaN layer) mounting substrate; and mounted on the mounting substrate., the mounting substrate has a depression which includes a reflective film on a wall thereof, (fig. 16) and the semiconductor light emitting device is mounted on a bottom of the depression, as a light source. (figs.14 -16 etc.)

With respect to claim 24 Durocher describes a manufacturing method for a semiconductor light emitting device, comprising the steps of:

forming a semiconductor multilayer structure including a light emitting layer on one of a plurality of main surfaces of a substrate; (fig. 4)

dividing the semiconductor multilayer structure into a plurality of portions each of which corresponds to a semiconductor light emitting device; (figs.l,13)

forming a phosphor film on and around each of the plurality of portions of the semiconductor multilayer structure; (figs. # 65, para 0097) and

dividing the substrate for each of the plurality of portions of the semiconductor multilayer structure. (figs. 1,13,) (this claim is the same as previously rejected claim 13).

With respect to claims 25 and 26 Durocher describes the method of Claim 24 further comprising the step of: varying a percentage of phosphor in the phosphor film to vary a color temperature of a white light emitted by the semiconductor light emitting device. and varying a thickness of the phosphor film to vary a color temperature of a white light emitted by the semiconductor light emitting device. (para 0067).

The limitations to vary a color temperature of a white light emitted by the semiconductor light emitting device is taken to be functional recitation and particular use recitation for which patentable weight cannot be given.

Response to Arguments

1. Applicant's arguments filed August 21, 2009 , have been fully considered but they are not persuasive for the following reasons:

Applicants' first contention that Durocer does not allegedly teach/describe ,

"[T]he plurality of light emitting elements are connected in series such that a cathode electrode of a light emitting element is connected to an anode electrode of a different light emitting element using a wire formed by a thin metal film formed on the insulating film." Is not persuasive because as stated in the rejection above

the plurality of light emitting elements are connected in series such that a cathode

electrode of a light emitting element is connected to an anode electrode of a different

light emitting element using a wire formed by a thin metal film formed , further Durocher

discloses on the insulating

film, (fig. 9- three LEDS fig. 9, figs. E.g. fig.1 connected to different LEDS , wire – figs.

E.g. fig. 10 # 61, 63 ,leads –well known to be formed from conductive metal on

insulating film figs. 16 # 38 etc.) (emphasis supplied).

Applicants' contention on page 11 that the LED chip is not conductive is not persuasive

because if the LED chip is not conductive how will it function as a LED and emit light?

Applicants' next argument is not commensurate in scope with the presently recited claim 1.

Applicants' are arguing a series connection between a set of LEDS is possible by connecting the first anode of the first LED to the cathode of the only last LED of the set. However the claim as presently recited also includes the [possibility of each LED of the set being connected to the next one in the set in series which allows to individual LED of the set to also have other connections ns as shown in Durocher.

5. Applicants' next contention that in fig.1, the LED chip through lead wire7, is not formed by a thin metal film, leads –well known to be formed from conductive metal.

Applicants' next contention that Durocher does not allegedly teach/disclose that the phosphor film covers at least the main surface of the semiconductor multilayer structure which faces away form the substrate since only portions of the semiconductor multilayer structure where the lighting elements 59 reside are covered is not persuasive because see for e.g. figure 11 (reproduced below):

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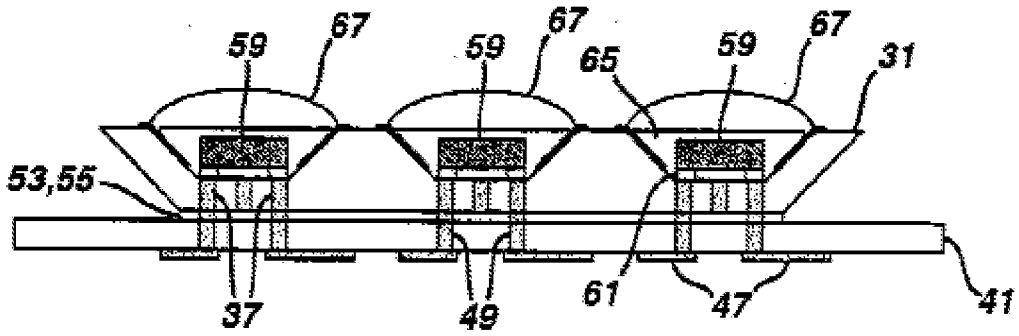
FIG. 11



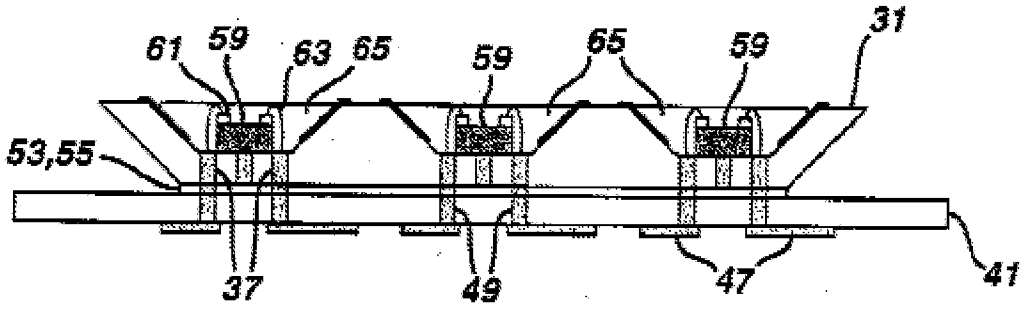
6.

As seen above phosphor film 67 covers the main surface of the semiconductor substrate 41 beyond LED 59.

Applicant' next contention wrt to claim 2 that allegedly DUricher does not teach/disclose "[T]he semiconductor multilayer structure includes a light reflective layer between the light emitting layer and the one of the plurality of main surface of the substrate. " is not persuasive because as stated in the rejection :

"the semiconductor light emitting device of Claim 1, wherein the semiconductor multilayer structure includes a light reflective layer between the light emitting layer and the one of the plurality of main surface of the substrate. (fig. 10 # 65 contacts top of 49 i.e. 65 is between 41- substrate and light emitting element 59 and see also claim 31, figs.) "

FIG. 10



7.

Applicants ' repeat their arguments under claim1 wrt to claim 24 and for arsons set out above and incorporated here by reference are not persuasive.

Applicants' arguments wrt to claims 27 and 28 are not persuasive for reasons set out above and further their arguments are commensurate in scope with presently recited claims, which are of different in scope their then the disclosure of figs. 4a and Band therefore also not persuasive.

Therefore all pending claims 2-7,14-21,25,26 and 28-40 are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN H. RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
Primary Examiner, Art Unit 2814

/Steven H Rao/
Examiner, Art Unit 2814

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